



(19)

**Europäisches Patentamt
European Patent Office
Office européen des brevets**



(11)

EP 0 477 809 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
17.12.1997 Bulletin 1997/51

(51) Int Cl. 6: **G06F 11/20**

(21) Application number: 91116107.3

(22) Date of filing: 21.09.1991

(54) High speed redundant rows and columns for semiconductor memories

Sehr schnelle redundante Zeilen und Spalten für Halbleiter-Speicher

Lignes et colonnes redondantes à haute vitesse pour mémoires à semi-conducteurs

(84) Designated Contracting States:
DE FR GB IT

(72) Inventor: Proebsting, Robert J.
Los Altos, California 94022 (US)

(30) Priority: 28.09.1990 US 590243

(74) Representative: Sparling Böhl Henseler

(43) Date of publication of application
01.04.1992 Bulletin 1992/14

Postfach 14 04 43
40074 Düsseldorf (DE)

(73) Proprietor: **Intergraph Corporation**
Huntsville, Alabama 35807-4201 (US)

Description

This invention relates to a semiconductor memory, according to the precharacterizing portion of claim 1.

Numerous types of semiconductor read/write memories such as SRAMs, DRAMs, PROMs, EEPROMs, etc., are well known and commercially available. Such memories are typically arranged as rows and columns of memory cells, each cell within which is capable of storing a single bit of information—a zero or a one.

With advances in integrated circuit fabrication technology, the number of memory cells which may be placed on a single chip is increasing rapidly. These advances result from two factors—the capability of integrated circuit manufacturers to manufacture reliably larger chips, and the shrinking size of memory cells enabling more cells to be placed in a given area.

To further enhance the yield of integrated circuit chips containing memory cells, redundant rows and columns of memory cells have been developed, and are now well known. (To simplify the following explanation, the term "columns" is used rather than "rows or columns." It will be appreciated that either or both rows or columns may be employed, even though only columns are mentioned.) In a typical memory having redundant columns, extra columns are included on the chip with the regular columns; however, the spare columns are fusibly or otherwise selectively connectible in place of defective columns. In typical prior art systems, fuses are used to disconnect a defective column and other fuses to electrically replace the defective column with the spare column, program the address decoder of the redundant column, and perform any other necessary changes.

Although such prior art systems function satisfactorily in the sense that it is transparent to the system in which the memory is employed whether the information accessed is stored in a regular column or in a spare column, the use of spare columns carries with it several disadvantages. The primary disadvantage of spare columns is access speed.

The spare columns typically are slower than regular columns because of signal propagation delays. Because the spare columns are located to one side or the other of the memory array, all of the regular columns in the memory array will have a relatively short path length connection to an output node, while the spare columns will have a longer path to get the output data from the physical location of the redundant column output to its required destination at the output of the defective column. The longer path delays signal transmission between the spare columns and the exterior of the chip as compared to the regular columns. Because the access time of a memory must take into account the time required to obtain data from the slowest column, these delays result in slower access time for circuits in which the spare columns are employed, as compared to circuits

in which they are not. The premium placed on high speed operation of memories makes this a substantial disadvantage.

US-A-4,691,301 shows a semiconductor memory adapted for use with a video RAM providing an array of memory elements arranged in rows and columns, wherein upon detection of a defective portion of the memory, an additional memory element, e.g. a column, is provided such that address changes within the memory can be avoided by providing a shift circuitry that allows to bypass the defective memory column and to append the additional memory column. To initialize the bypass, two fuses have to be blown in a first step; subsequently, a further fuse in a reconfiguration logic has to be opened for shifting the voltage applied to switches which is applied to the lines that include the first mentioned two fuses. Further, a deactivation circuit fuse provided with each of the memory elements has to be blown to disable the input of the respective driver, thus allowing it to float.

Starting from a semiconductor memory according to the precharacterizing portion of claim 1, it is the object of the invention to provide an improved semiconductor memory that allows redundant columns that are as fast as the other columns to be replaced in an easy and fast manner.

This object is achieved by the features of the characterizing clause of claim 1.

The invention provides a memory system in which redundant columns may be employed without diminishing the speed of operation of the overall integrated circuit in which they are employed. The spare columns employed according to this invention do not have increased propagation delay, and therefore access time, as compared to the regular columns. The avoidance of extra propagation delay for the spare columns is made possible by a unique switching system in which every column input/output node is selectively connectible by a short path length connection to more than one input/output line in the array. By not connecting a defective column to any input/output line, memories only use good columns and will operate at the same speed whether or not any defective, but unused, columns exist.

An embodiment of the invention will now be illustrated with reference to the appended drawing.

Figure 1 is a block diagram illustrating the operating principle of the invention.

Figure 2 is a circuit schematic illustrating a detailed embodiment of the invention.

Figure 1 is a block diagram which illustrates the operating principle of the invention. Shown in Figure 1 are columns of memory cells arbitrarily designated a, b, c, d, Each column of memory cells is intended to represent a series of cells connected along a single column. Typically, the column length will be a number of cells which is a power of two, for example, 256. Each of the cells is connected in a well known manner, so that when suitable addressing information is supplied on a row

connected to the particular cell, the data supplied through the column can be written onto the memory cell or the contents of the cell can be detected and read out through the column connections. For this reason lines 1, 2, 3, . . . n are referred to herein as input/output lines. Of course, in other embodiments of the invention where redundant rows are employed in place of defective rows, the columns shown in Figure 1 may be considered to be rows.

Each of the columns (or rows) has an input/output connection A, B, C, D, . . . , as illustrated. Ultimately, the columns are to be connected to input/output lines 1, 2, 3, 4, . . . , also as shown. Each of the input/output lines has associated with it a corresponding switch. For example, input/output line 1 has connected to it a switch 11. Input/output line 2 has a switch 12 connected to it. Input/output line 3 includes a switch 13. As shown the switches allow an input/output line to be connected to either one of two columns of memory cells.

To understand the function of the switches in replacing a defective column of memory cells with a redundant functional column, assume that column d is defective. Column d can be switched out of operation, and a functional column switched in its place, by appropriate positioning of the switches. To achieve this, switch 11 is positioned to connect line 1 to node A. Switch 12 is employed to connect line 2 to node B. Switch 13 connects line 3 to node C. Now, instead of connecting line 4 to node D, switch 14 is used to connect line 4 to node E. Similarly, switch 15 is used to connect line 5 to node F. As will be appreciated, by having positioned all of the switches on the left side of the defective column to connect to columns to the left of their respective input/output connections, and by positioning all of the switches on the right side of the defective column to connect to the columns on the right side of their respective input/output connections, the defective column is removed from operation without increase in propagation delays. In particular, the signal path length between each of the input/output lines 1, 2, 3, 4, and 5 and the corresponding column connections A, B, C, E, and F is of equal length and therefore equal delay.

The preceding discussion assumes that for each column of memory cells only a single input/output line is required. For embodiments of the invention applicable to memories employing complementary input/output lines, such as the complementary bit lines in conventional DRAMs and SRAMs, each of the nodes A, B, . . . , represent a pair of column connections, while each switch 11, 12, . . . , represents a pair of switches, and each line 1, 2, . . . , represents a pair of lines. For such an embodiment the connections among the switches, input/output lines and nodes are discussed below.

A preferred embodiment for the circuitry for implementing the switches 11, 12, . . . with CMOS technology is shown in Figure 2. The circuitry depicted there illustrates the implementation of the switches for both single bit line and complementary bit line embodiments. The

single bit line embodiment uses only one single-pole, double-throw switch per input/output bit, e.g., switch 13 for input/output line 3 and switch 14 for input/output line 4. For the complementary bit line embodiment both the true and complementary switches are used, i.e., switch 13 is used for line 3 and switch 13' is used for line 3'. Switch 13 can be set to connect input/output bit 3 to either column C or to column D and is set to connect input/output line 3 to column connection C, while switch 14 is set to connect input/output line 4 to column E.

The circuitry shown in Figure 2 is connected to a potential source Vcc, typically +5 volts, which is applied to line 20. Line 20 also includes a series of fuses 21, 22, with one fuse being disposed between each pair of switches as shown. For example, fuse 22 separates switch pair 13, 13' from switch pair 14, 14'.

Each switch includes two pairs of complementary MOS transistors. PMOS transistors are designated by a small circle on their gates. For example, switch 13 includes an NMOS transistor 31, a PMOS transistor 32, a second NMOS transistor 33, and a second PMOS transistor 34. Each of the complementary pairs of transistors has correspondingly connected sources and drains as shown. That is, transistors 31 and 32 have their sources coupled together, and their drains coupled together, as do transistors 33 and 34. In addition, line 37 connects the gate of transistor 31 to the gate of transistor 34, while line 38 connects the gate of transistor 32 to the gate of transistor 33. Line 37 is connected directly to node 20', while line 38 is connected to the output of inverter 40 whose input is node 20'.

Switch 14 is similar in structure to switch 13. Switch 14 also includes two pairs of transistors configured to connect input/output line 4 to one of nodes D or E. Node 57 in switch 14 corresponds to node 37 in switch 13, while node 58 in switch 14 corresponds to node 38 in switch 13.

The state of the switches 13 and 14 is controlled by fuses in the line 20. Because fuse 21 and all fuses (not shown) to the left of fuse 21 have not been blown, line 37 will be connected directly to the positive voltage Vcc holding NMOS transistor 31 on and PMOS transistor 34 off. Inverter 40 will cause an opposite condition on line 38, turning on PMOS transistor 32 and turning off NMOS transistor 33. Hence, both transistors 31 and 32 will be on, while both transistors 33 and 34 will be off. The on condition of both transistors 31 and 32 connects column connection C to input/output line 3. Similarly, the off condition of both transistors 33 and 34 disconnects input/output line 3 from column connection D. As a result, input/output line 3 is connected only to column connection C. In a corresponding manner, all of the switches (not shown) to the left of switch 13 will be switched to the left (as shown in Figure 1).

A resistor 62 is connected between the right side of line 20 and ground. Its purpose is to bring all nodes 20, 20', 20", etc., to the right of any single blown fuse element to ground rather than to Vcc. All of the switches to

the right of fuse 22 are thrown to the right by virtue of the blowing of fuse 22. Fuse 22 will be blown at the time the memory circuit is tested, and may be blown using any well known technique. In a preferred embodiment, a laser is employed. Opening fuse 22 allows resistor 62 to bring those portions of line 20 to the right of the blown fuse element 22 to ground. The low level on line 20" is directly connected to line 57, thereby turning off NMOS transistor 51 and turning on PMOS transistor 54. Inverter 60 supplies a high potential to line 58, thereby turning off PMOS transistor 52 and turning on NMOS transistor 53. The on condition of both transistors 53 and 54 connects input/output line 4 to column connection E. Correspondingly, the off condition of transistors 51 and 52 disconnects column connection D from input/output line 4. Because each of transistors 33, 34, 51 and 52 is off, node D is isolated, and defective memory cell column D is disconnected from all input/output lines.

At the bottom of Figure 2, an additional pair of switches 13' and 14' are depicted. These switches are added for semiconductor read/write memories employing complementary input/output lines, for example, most SRAMs and DRAMs. Each of the complementary input/output line switches 13' and 14' is identical, with respect to its internal circuitry, to the corresponding switches 13 and 14. Each complementary bit line switch 13', 14' is also connected to line 20. In the manner depicted, however, instead of being connected to the true column connections C, D, and E, the complementary bit line switches are connected to nodes \bar{C} , \bar{D} and \bar{E} . The complementary switches provide complementary input/output nodes $\bar{3}$ and $\bar{4}$ in the same manner as the true input/output line switches provide input/output nodes 3 and 4.

Although a preferred embodiment of the invention has been described above with respect to specific circuitry, it should be understood that the invention is not so limited. Other circuits may be readily employed to carry out the invention using different switching arrangements. For example, bipolar switches may be employed. In addition, while fuses have been described as a preferred embodiment for turning off and on the various switches, it should be appreciated that any technique may be employed for connecting and disconnecting the line as necessary, for example, PROM or EPROM cells.

Claims

1. A semiconductor memory comprising:

a first plurality of columns (c, d, e) of memory cells, each column having a corresponding input/output node means (C, D, E; \bar{C} , \bar{D} , \bar{E}) coupled to the column; a second plurality of input/output line means (3, 4; $\bar{3}$, $\bar{4}$), the second plurality being less than the first plurality, each input/output line means (3,

5 4; $\bar{3}$, $\bar{4}$) having corresponding connection node means; and a third plurality of switch means (13, 14; 13', 14'), the third plurality being of the same number as the second plurality, each switch means (13, 14; 13', 14') being connected to a corresponding connection node means of the second plurality of input/output line means (3, 4; $\bar{3}$, $\bar{4}$), and being selectively connectible to one of at least two of the input/output node means (C, D, E; \bar{C} , \bar{D} , \bar{E}) of adjoining columns (c, d, e) of memory cells, a fourth plurality of fuses (22) provided in a common conducting line (20), each of said fuses (22) delimiting nodes (20', 20") of said common conducting line (20), each of said third plurality of switch means (13, 14; 13', 14') being connected to one corresponding node (20', 20") characterized in that the common conducting line (20) is coupled between a power supply potential (V_{cc}) and a reference potential (ground) such that when a single fuse (22) is blown all switch means (13'; 14') on one side of the blown fuse connect to a first portion (C; \bar{C}) of the input/output nodes, and all switch means (14; 14') on the other side of the blown fuse (22) connect to a second portion (E; \bar{E}) of the input/output nodes to thereby eliminate any connection to a defective column (d) located between the first and second portions.

20 2. A memory according to claim 1, wherein each switch means (13; 13') is selectively connectible to one of two of the input/output node means (C, D; \bar{C} , \bar{D}).

25 3. A memory according to claim 1 or 2, characterized in that each switch means (13, 14) comprises first transistor means (31, 32; 51, 52) to connect or disconnect a selected input/output line (3; $\bar{3}$; 4; $\bar{4}$) from the input/output node (C; \bar{C} ; D; \bar{D}) of a first adjoining column of memory cells and second transistor means (34, 33; 54, 53) to connect or disconnect the selected input/output line (3; $\bar{3}$; 4; $\bar{4}$) from the input/output node (D, \bar{D} ; E, \bar{E}) of a second adjoining column of memory cells.

30 4. A memory according to claim 3, characterized in that the first transistor means comprises a pair (31, 32; 51, 52) of complementary field effect transistors connected together, and that the second transistor means comprises a pair (34, 33; 54, 53) of complementary field effect transistors connected together.

35 5. A memory according to claim 4, characterized in

40 that the first pair of complementary field effect transistors includes a first PMOS transistor (32;

45

50

55

52) and a first NMOS transistor (31; 51),
 that the second pair of complementary field effect transistors includes a second PMOS transistor (34; 54) and a second NMOS transistor (33; 53),
 that a control electrode of the first PMOS transistor (32; 52) and a control electrode of the second NMOS transistor (33; 53) are connected together at a first node (38; 58),
 that a control electrode of the second PMOS transistor (34; 54) and a control electrode of the first NMOS transistor (31; 51) are connected together at a second node (37; 57),
 that connecting means are provided for connecting one of the first (38; 58) and second (37; 57) nodes to a potential (V_{cc}), and
 that inverting means (40; 60) for achieving an opposite state are connected between the one and the other of the first and second nodes to maintain them in opposite states.

6. A semiconductor according to one of claims 1 to 5, characterized in that the common conducting line (20) is connected to a potential source (V_{cc}), that a resistor (62) is connected between the common conducting line (20) and ground, and that the fuses are disposed in series between the potential source (V_{cc}) and the resistor (62).

7. A memory according to claim 6, characterized in that the potential of the potential source (V_{cc}) is applied to the switch means on one side of the blown fuse while ground is applied to the switch means on the other side of the blown fuse.

8. A memory according to one of claims 1 to 7, characterized in that each input/output node means comprises one node, that each input/output line means comprises one input/output line, that each connection node means comprises one connection node, and that each switch means comprises one switch.

9. A memory according to one of claims 1 to 7, characterized in that each of the columns of memory cells includes a pair of lines,
 that each of the input/output node means comprises a pair of input/output nodes (C, \bar{C} ; D, \bar{D} ; E, \bar{E}), one coupled to each of the pair of lines,
 that each of the input/output line means comprises a pair of input/output lines (3, $\bar{3}$; 4, $\bar{4}$),
 that each connection node means comprises a pair of connection nodes, one coupled to each of the pair of input/output lines, and
 that each switch means comprises a pair of switches (13, 13'; 14, 14'), one coupled to each of the connection nodes.

10. A memory according to one of claims 1 to 9, characterized in that the fourth plurality of fuses (22) is of the same number than the third plurality of switch means (13, 14; 13', 14'), and that the fuses are capable to be blown by a laser beam.

10 Patentansprüche

1. Halbleiterspeicher, umfassend:

eine erste Mehrzahl von Spalten (c, d, e) von Speicherzellen, wobei jede Spalte ein entsprechendes Eingangs-/Ausgangsknotenmittel (C, D, E; \bar{C} , \bar{D} , \bar{E}) hat, das an die Spalte angekoppelt ist,
 eine zweite Mehrzahl von Eingangs-/Ausgangsleitungsmitteln (3, 4; $\bar{3}$, $\bar{4}$), welche zweite Mehrzahl kleiner ist als die erste Mehrzahl, wobei jedes Eingangs-/Ausgangsleitungsmittel (3, 4; $\bar{3}$, $\bar{4}$) zugeordnete Anschlußknotenmittel hat, und
 eine dritte Mehrzahl von Schaltermitteln (13, 14; 13', 14'), welche dritte Mehrzahl die gleiche Anzahl hat wie die zweite Mehrzahl, wobei jedes Schaltermittel (13, 14; 13', 14') mit einem entsprechenden Anschlußknotenmittel der zweiten Mehrzahl von Eingangs-/Ausgangsleitungsmitteln (3, 4; $\bar{3}$, $\bar{4}$) verbunden ist, und selektiv anschließbar ist an eine von mindestens zwei der Eingangs-/Ausgangsknotenmittel (C, D, E; \bar{C} , \bar{D} , \bar{E}) anschließender Spalten (c, d, e) von Speicherzellen,
 eine vierte Mehrzahl von Schmelzkörpern (22), die in einer gemeinsamen leitenden Leitung (20) vorgesehen ist, wobei jeder der Schmelzkörper (22) Knoten (20', 20'') der gesamten leitenden Leitung (20) begrenzt, wobei jeder der dritten Mehrzahl von Schaltermitteln (13, 14; 13', 14') mit einem entsprechenden Knoten (20', 20'') verbunden ist, dadurch gekennzeichnet, daß die gemeinsame leitende Leitung (20) zwischen ein Leistungsversorgungspotential (V_{cc}) und ein Referenzpotential (Masse) gekoppelt ist, derart, daß dann, wenn ein einzelner Schmelzkörper (22) durchgeschmolzen wird, alle Schaltermittel (13; 14') auf einer Seite des durchgeschmolzenen Schmelzkörpers mit einem ersten Abschnitt (C; C) der Eingangs-/Ausgangsknoten verbunden werden und alle Schaltermittel (14; 14') auf der anderen Seite des aufgeschmolzenen Schmelzkörpers (22) mit einem zweiten Abschnitt (E; \bar{E}) der Eingangs-/Ausgangsknoten verbunden werden, um dadurch jede Verbindung mit einer defekten Spalte zu eliminieren, die sich zwischen dem

ersten und dem zweiten Abschnitt befindet.

2. Speicher nach Anspruch 1, bei dem jedes Schaltermittel (13; 13') selektiv mit einem der beiden Eingangs-/Ausgangsknotenmittel (C, D; \bar{C} , \bar{D}) verbindbar ist.

3. Speicher nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß jedes Schaltermittel (13, 14) erste Transistormittel (31, 32; 51, 52) umfaßt, um eine ausgewählte Eingangs-/Ausgangsleitung (3; $\bar{3}$; 4; $\bar{4}$) mit dem Eingangs-/Ausgangsknoten (C; \bar{C} ; D; \bar{D}) einer ersten anschließenden Spalte von Speicherzellen zu verbinden bzw. die Verbindung zu unterbrechen, und zweite Transistormittel (34, 33; 54, 53) umfaßt, um die ausgewählte Eingangs-/Ausgangsleitung (3; $\bar{3}$; 4; $\bar{4}$) mit dem Eingangs-/Ausgangsknoten (D, \bar{D} ; E, \bar{E}) einer zweiten anschließenden Spalte von Speicherzellen zu verbinden bzw. die Verbindung zu unterbrechen.

4. Speicher nach Anspruch 3, dadurch gekennzeichnet, daß die ersten Transistormittel ein Paar (31, 32; 51, 52) von miteinander verbundenen komplementären Feldeffekttransistoren umfassen, und daß die zweiten Transistormittel ein Paar miteinander verbundener komplementärer Feldeffekttransistoren (34, 33; 54, 53) umfassen.

5. Speicher nach Anspruch 4, dadurch gekennzeichnet,

daß das erste Paar komplementärer Feldeffekttransistoren einen ersten PMOS Transistor (32; 52) und einen ersten NMOS Transistor (31; 51) umfaßt,

daß das zweite Paar von komplementären Feldeffekttransistoren einen zweiten PMOS Transistor (34; 54) und einen zweiten NMOS Transistor (33; 53) umfaßt,

daß eine Steuerelektrode des ersten PMOS Transistors (32; 52) und eine Steuerelektrode des zweiten NMOS Transistors (33; 53) miteinander an einem ersten Knoten (38; 58) verbunden sind,

daß eine Steuerelektrode des zweiten PMOS Transistors (34; 54) und eine Steuerelektrode des ersten NMOS Transistors (31; 51) miteinander an einem zweiten Knoten (37; 57) verbunden sind,

daß Verbindungsmitte für das Verbinden eines der ersten (38; 58) und zweiten (37; 57) Knoten mit einem Potential (V_{cc}) vorgesehen sind, und daß Invertiermittel (40; 60) für das Erreichen eines entgegengesetzten Zustands zwischen den einen und anderen der ersten und zweiten Knoten geschaltet sind, um sie in entgegengesetzten Zuständen zu halten.

6. Speicher nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß die gemeinsame leitende Leitung (20) mit einer Potentialquelle (V_{cc}) verbunden ist, daß ein Widerstand (62) zwischen die gemeinsame leitende Leitung (20) und Masse geschaltet ist und daß die Schmelzkörper in Serie zwischen die Potentialquelle (V_{cc}) und den Widerstand (62) gelegt sind.

7. Speicher nach Anspruch 6, dadurch gekennzeichnet, daß das Potential der Potentialquelle (V_{cc}) an die Schaltermittel auf einer Seite des aufgeschmolzenen Schmelzkörpers angelegt ist, während Masse an die Schaltermittel auf der anderen Seite des aufgeschmolzenen Schmelzkörpers angelegt ist.

8. Speicher nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß jedes Eingangs-/Ausgangsknotenmittel einen Knoten umfaßt, daß jedes Eingangs-/Ausgangsleitungsmittel eine Eingangs-/Ausgangsleitung umfaßt, daß jedes Verbindungsmitte einen Verbindungsknoten umfaßt, und daß jedes Schaltermittel einen Schalter umfaßt.

9. Speicher nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet,

daß jede der Spalten von Speicherzellen ein Paar von Leitungen umfaßt,

daß jedes der Eingangs-/Ausgangsknotenmittel ein Paar von Eingangs-/Ausgangsknoten (C, \bar{C} ; D, \bar{D} ; E, \bar{E}) umfaßt, von denen einer mit jedem Paar von Leitungen gekoppelt ist,

daß jedes der Eingangs-/Ausgangsleitungsmittel ein Paar von Eingangs-/Ausgangsleitungen (3; $\bar{3}$; 4; $\bar{4}$) umfaßt,

daß jedes Verbindungsmitte ein Paar von Verbindungsknoten umfaßt, einer angekoppelt an jede aus dem Paar von Eingangs-/Ausgangsleitungen, und

daß jedes Schaltermittel ein Paar von Schaltern (13, 13'; 14, 14') umfaßt, einer angekoppelt an jeden der Anschlußknoten.

10. Speicher nach einem der Ansprüche 1 bis 9, dadurch gekennzeichnet, daß die vierte Mehrzahl von Schmelzkörpern (22) die gleiche Anzahl aufweist wie die dritte Mehrzahl von Schaltermitteln (13, 14; 13', 14'), und daß die Schmelzkörper ausgebildet sind, um durch einen Laserstrahl aufgeschmolzen zu werden.

Revendications

1. Mémoire à semi-conducteurs comprenant :

une première pluralité de colonnes (c,d,e) de

cellules mémoire, chaque colonne ayant des moyens de noeud d'entrée/sortie correspondant (C,D,E ; \bar{C} , \bar{D} , \bar{E}) couplé à la colonne ; une seconde pluralité de moyens de ligne d'entrée/sortie (3,4 ; $\bar{3}$, $\bar{4}$), la seconde pluralité étant inférieure à la première pluralité, chaque moyen de ligne d'entrée/sortie (3, 4 ; $\bar{3}$, $\bar{4}$) ayant des moyens de noeud de connexion correspondants ; et une troisième pluralité de moyens de commutation (13, 14 ; 13', 14'), la troisième pluralité étant numériquement égale à la seconde pluralité, chaque moyen de commutation (13, 14 ; 13', 14') étant connecté à un moyen de noeud de connexion correspondant de la seconde pluralité de moyens de ligne d'entrée/sortie (3, 4 ; $\bar{3}$, $\bar{4}$), et étant sélectivement apte à être connecté à l'un d'au moins deux des moyens de noeud d'entrée/sortie (C, D, E; \bar{C} , \bar{D} , \bar{E}) des colonnes adjacentes (c,d,e) de cellules mémoire,

une ligne de connexion commune (20) est couplée entre une alimentation de tension (Vcc) et un potentiel de référence (masse), une quatrième pluralité de fusibles (22) étant prévue dans la ligne conductrice commune (20), chacun desdits fusibles (22) délimitant des noeuds (20', 20'') de ladite ligne conductrice commune (20), chacun des moyens de commutation (13,14 ; 13', 14') de ladite troisième pluralité étant connecté à un noeud correspondant (20', 20''), caractérisée en ce que lorsqu'un fusible unique (22) est fondu, tous les moyens de commutation (13', 14') d'un côté du fusible fondu se connectent à une première partie (C, \bar{C}) des noeuds d'entrée/sortie, et tous les moyens de commutation (14, 14') de l'autre côté du fusible fondu (22) se connectent à une seconde partie (E, \bar{E}) des noeuds d'entrée/sortie pour ainsi éliminer toute connexion à une colonne défectueuse (d) située entre les premières et secondes parties.

2. Mémoire selon la revendication 1, dans laquelle chaque moyen de commutation (13, 13') est sélectivement connectable à l'un parmi deux des moyens de noeud d'entrée/sortie (C,D ; \bar{C},\bar{D}).

3. Mémoire selon la revendication 1 ou 2, caractérisée en ce que chaque moyen de commutation (13, 14) comporte des premiers moyens de transistor (31,32 ; 51,52) pour connecter ou déconnecter une ligne d'entrée/sortie sélectionnée (3, $\bar{3}$; 4, $\bar{4}$) par rapport au noeud d'entrée/sortie (C ; \bar{C} ; D ; \bar{D}) d'une première colonne adjacente de cellules mémoire et des seconds moyens de transistor (34, 33 ; 54, 53) pour connecter ou déconnecter la ligne d'en-

trée/sortie sélectionnée (3, $\bar{3}$; 4, $\bar{4}$) par rapport au noeud d'entrée/sortie (D, \bar{D} ; E, \bar{E}) d'une seconde colonne adjacente de cellules mémoire.

5. 4. Mémoire selon la revendication 3, caractérisée en ce que les premiers moyens de transistor comportent une paire (31, 32 ; 51, 52) de transistors complémentaires à effet de champ connectés ensemble, et en ce que les seconds moyens de transistors comportent une paire (34, 33 ; 54, 53) de transistors complémentaires à effet de champ connectés ensemble.

5. Mémoire selon la revendication 4, caractérisée en ce que la première paire de transistors complémentaires à effet de champ comporte un premier transistor PMOS (32, 52) et un premier transistor NMOS (31, 51),

en ce que la seconde paire de transistors complémentaires à effet de champs comporte un second transistor PMOS (34, 54) et un second transistor NMOS (33, 53),

en ce qu'une électrode de commande du premier transistor PMOS (32,52) et une électrode de commande du second transistor NMOS (33 ; 53) sont connectées ensemble à un premier noeud (38, 58),

en ce qu'une électrode de commande du second transistor PMOS (34, 54) et une électrode de commande du premier transistor NMOS (31, 51) sont connectées ensemble à un second noeud (37, 57),

en ce que des moyens de connexion sont prévus pour connecter l'un des premiers noeuds (38, 58) et l'un des seconds noeuds (37, 57) à un potentiel (Vcc), et

que des moyens d'inversion (40 ; 60) pour obtenir un état opposé sont connectés entre l'un et l'autre des premiers et seconds noeuds pour les maintenir dans des états opposés.

6. Semi-conducteur selon l'une des revendications 1 à 5, caractérisé en ce que la ligne conductrice commune (20) est connectée à une source de potentiel (Vcc), qu'une résistance (62) est connectée entre la ligne conductrice commune (20) et la masse, et que les fusibles sont disposés en série entre la source de potentiel (Vcc) et la résistance (62).

7. Mémoire selon la revendication 6, caractérisée en ce que le potentiel de la source de potentiel (Vcc) est appliqué aux moyens de commutation sur un côté du fusible fondu, alors que la masse est appliquée aux moyens de commutation de l'autre côté du fusible fondu.

8. Mémoire selon l'une des revendications 1 à 7, ca-

ractérisée en ce que chaque moyen de noeud d'entrée/sortie comporte un noeud, que chaque moyen de ligne d'entrée/sortie comporte une ligne d'entrée/sortie, que chaque moyen de noeud de connexion comporte un noeud de connexion, et que chaque moyen de commutation comporte un commutateur. 5

9. Mémoire selon l'une des revendications 1 à 7, caractérisée en ce 10

que chacune des colonnes de cellules mémoire comporte une paire de lignes, que chacun des moyens de noeuds d'entrée/sortie comporte une paire de noeuds d'entrée/sortie (C, \bar{C} ; D, \bar{D} ; E, \bar{E}) chaque noeud étant couplé à chacune des paires de lignes, que chacun des moyens de ligne d'entrée/sortie comporte une paire de lignes d'entrée/sortie (3 ; $\bar{3}$; 4 ; $\bar{4}$), 20 que chacun des moyens de noeud de connexion comporte une paire de noeuds de connexion, chaque noeud étant couplé à chacune des paires de lignes d'entrée/sortie, et que chaque moyen de commutation comporte 25 une paire de commutateurs (13, 13'; 14 ; 14'), chaque commutateur étant connecté à chacun des noeuds de connexion.

10. Mémoire selon l'une des revendications 1 à 9, caractérisée en ce que la quatrième pluralité de fusibles (22) est numériquement égale à la troisième pluralité de moyens de commutation (13, 14 ; 13', 14'), et en ce que les fusibles sont aptes à être fondu par un faisceau laser. 30 35

40

45

50

55

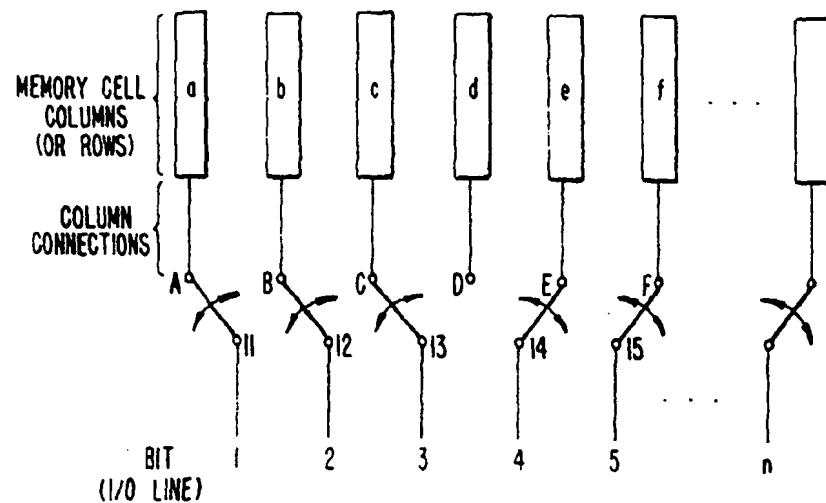


FIG. 1.

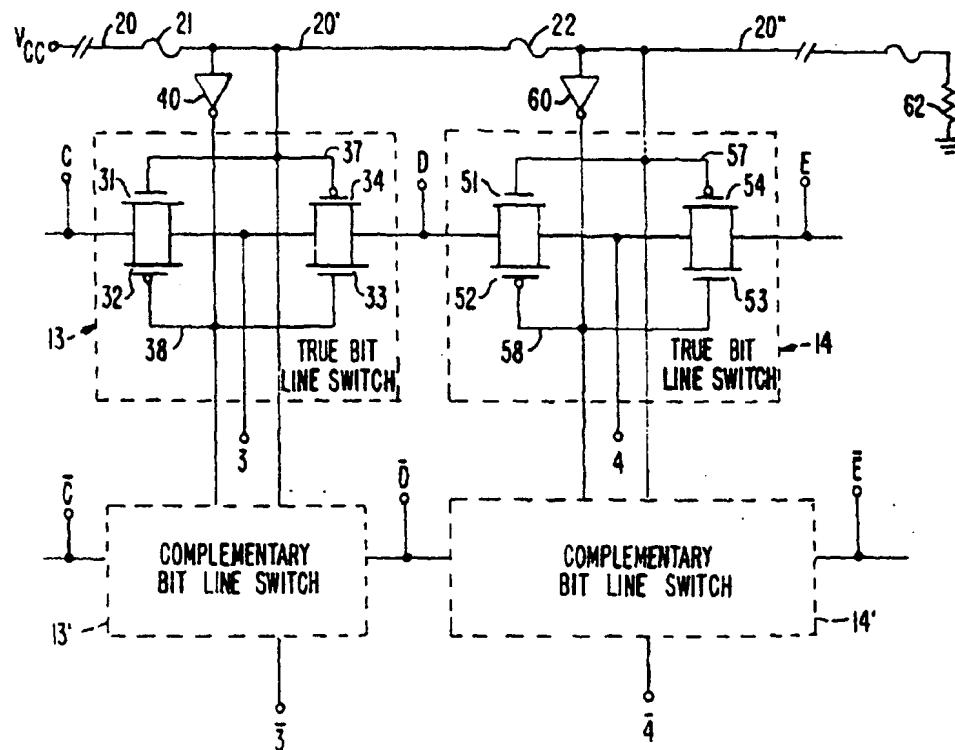


FIG. 2.